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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,908	09/29/2003	Sunil Kumar Sharma	11556(P-54)USA; 2110-80-3	2081

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,908	SHARMA, SUNIL KUMAR	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-12* is/are allowed.

6)☒ Claim(s) *1,2,4-7,13,15-18 and 20* is/are rejected.

7)☒ Claim(s) *3,14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 17-20 are objected to because of the following informalities:

I. Claims 17-19 need a comma after 16.

II. Claim 20 should have ", wherein" after 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 4, and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 1, 4, and 7 recite the limitation "the mapping constraints". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-7, 13, 15-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaviani (US Patent 6,212,670).

5. As for claims 1-2, 4-7, 13, 15-18, and 20, Kaviani discloses the invention as claimed, including an improved method/(electronic)system for mapping an electronic digital circuit to a look up table (LUT) based programmable logic device (PLD) comprising the steps of:
Selecting an unmapped or partially mapped LUT [col. 2, lines 18-22; col. 7, lines 26-45];
Identifying a group of circuit elements for mapping based on the available capacity of the selected LUT and the mapping constraints [col. 2, lines 18-22; col. 7, lines 26-45];
Mapping the group of circuit elements onto the selected LUT [col. 2, lines 18-22; col. 7, lines 26-45]; and
Continuing the process of selecting an LUT, forming a group of ciruit elements and mapping until all the circuit elements have been mapped [col. 2, lines 18-22; col. 7, lines 26-45; col. 8, lines 60-61 – the goal of implementing the circuit is accomplished by completing the mapping process];
Characterized in that, the cascade logic associated with each LUT is also incorporated in the steps of forming the group of circuit elements and the mapping of the group [col. 2, lines 18-22; col. 7, lines 26-45].
Wherein the group of circuit elements are mapped to he cascade logic prior to mapping the LUTs [col. 2, lines 18-22; col. 7, lines 26-45 – it is decided prior to mapping, what cascade elements are needed to implement the circuit];
Wherein the mapping constraints include timing, placement and size constraints [col. 7, lines 27-45, especially lines 32-36 – the minimizing area and speed of operation read on timing, placement, and area; the minimization of area constraint incorporates placement and size constraints in order to do a minimization];
Wherein the mapping on the cascade logic incorporates at least one or more of the following constraints/verification depending on the connectivity of the architecture; XOR, XNOR, and NOT functions are not mapped on the cascade logic [col. 1, shows logic

elements that do not include XOR, XNOR, and NOT functions that are mapped to the PLA-like circuits];
A method for programming a PLD including LUTs and cascade elements, the method comprising:
Mapping logic into LUTs [col. 2, lines 18-22; col. 7, lines 26-45];
Mapping logic into cascade elements [col. 2, lines 18-22; col. 7, lines 26-45];
Repeating the operations of mapping logic into the LUTs and mapping logic into the cascade elements until all logic has been mapped into the PLD [col. 2, lines 18-22; col. 7, lines 26-45; col. 8, lines 60-61 – the goal of implementing the circuit is accomplished by completing the mapping process];
Mapping is done in accordance with timing, placement, and size constraints [col. 7, lines 27-45, especially lines 32-36 – the minimizing area and speed of operation read on timing, placement, and area; the minimization of area constraint incorporates placement and size constraints in order to do a minimization];
An FPGA [col. 1];
A computer system [col. 6, lines 51-54];
Each PLD comprises logic block circuitry, I/O circuitry, and routing channel circuitry [figs. 1-3].

6. Claims 8-12 are allowed over the prior art of record.

7. Claims 3, 14, and 19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination, the invention as claimed, including wherein the cascade logic is incorporated only after either all circuit elements have initially been mapped onto LUTs or some circuit elements remain unmapped even after all LUTs have been utilized; the determining

steps of mapping cascade elements of claim 8; the combination of steps of claim 14; and the mapping step of claim 19.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
October 17, 2005